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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,947	03/27/2001	Shigetsugu Muramatsu	78-01	9848

7590 09/24/2002

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EXAMINER
NORRIS, JEREMY C

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,947	MURAMATSU ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 6-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 6-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 2-4 and 6-20 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,392,160, granted to Andry et al. (hereafter Andry).

Andry discloses a substrate for mounting an electronic part (22-1) or parts thereon comprising a core substrate (40D-1 et al.) and at least a set of insulation layer (48) and a patterned wiring line layer (44G-N) which is formed on the insulation layer, said set of insulation layer and patterned wiring line layer being positioned at at least one of two opposed sides of the core substrate, the core substrate having holes (39), in each of which a lead pin of the electronic part is to be inserted, and said core substrate being provided with lands which surround an opening of each of the holes and to which the lead pin inserted in the hole is to be bonded, wherein the insulation layer or insulation layers located at at least one side of the core substrate has bores (47), which expose the land at a bottom of the bores, and communicate with the holes; wherein the

holes, in which the lead pin of the electronic part is to be inserted, have a closed end at the side of the core substrate opposed to the side on which the electronic parts are to be mounted [claims 6, 13-15], wherein the hole, in which the lead pin of the electronic part is to be inserted, has an inside wall on which a conductor layer is formed, the conductor layer being led to the land [claim 2], further comprising lands which surround the opening of the hole at the side of the core substrate opposed to the side on which the electronic parts are to be mounted, and which are led to the conductor layer on the inside wall of the hole [claim 3], wherein the land at the side of the core substrate opposed to the side on which the electronic parts are mounted is connected to a wiring line at this side [claim 4], wherein the closed end is closed by the insulation layer on the core substrate [claim 8], wherein a wiring line (49) is provided on the insulation layer at an area corresponding to the location of the hole with the closed end [claim 10], further comprising a hole (39) piercing through the core substrate and having an inside wall on which a conductor layer is provided to connect a wiring line at one side of the core substrate to another wiring line at the opposed side [claim 12]

Andry additionally discloses, referring to figure 1A, a substrate for mounting an electronic part (22-1) or parts thereon comprising a core substrate (40D-1 et al.) and at least a set of insulation layer (48) and a patterned wiring line layer (44G-N) which is formed on the insulation layer, said set of insulation laver and patterned wiring, line layer being positioned at at least one of two opposed sides of the core substrate, the core substrate having holes (39), in each of which a lead pin of the electronic part is to be inserted, and said core substrate being provided with lands which surround an

opening of each of the holes and to which the lead pin inserted in the hole is to be bonded, wherein the insulation layer or insulation layers located at at least one side of the core substrate has bores (47), which expose the land at a bottom of the bores, and communicate with the holes; wherein at least one of the holes, in which the lead pin of the electronic part is to be inserted, has an open end at the side of the core substrate opposed to the side on which the electronic parts are to be mounted (see fig. 3A), and at least one of the holes, in which the lead pin of the electronic part is to be inserted, has a closed end at the side of the core substrate opposed to the side on which the electronic parts are to be mounted [claim 7], wherein the closed end is closed by the insulation layer on the core substrate [claim 9], wherein a wiring line (49) is provided on the insulation layer at an area corresponding to the location of the hole with the closed end [claim 11], wherein the hole, in which the lead pin of the electronic part is to be inserted, has an inside wall on which a conductor layer is formed, the conductor layer being led to the land [claim 16], further comprising lands which surround the opening of the hole at the side of the core substrate opposed to the side on which the electronic parts are to be mounted, and which are led to the conductor layer on the inside will of the hole [claim 17], wherein the land at the side of the core substrate opposed to the side on which the electronic parts are to be mounted is connected to a wiring line at said side [claim 18], further comprising a hole (39) piercing through the core substrate and having an inside wall on which a conductor layer is provided to connect a wiring line at one side of the core substrate to another wiring line at the opposed side [claim 19].

Moreover, Andry discloses, referring to figure 1A, a substrate for mounting an electronic part (22-1) or parts thereon, comprising a core substrate (40D-1 et al.) and at least a set of insulation layer (48) and patterned wiring line layer (44G-N), which is formed on the insulation layer, at opposed sides of the core substrate, the core substrate having holes (39), in each of which a lead pin of the electronic part to be mounted is to be inserted, and being provided with lands which surround an opening of the hole and to which the lead pin inserted in the hole is to be bonded, and holes having an inside wall on which a conductor layer is formed, the conductor layer extending to a land provided on each of the sides of the core substrate in order to connect a wiring line at one side of the core substrate to another wiring line at the opposed side, wherein the insulation laver or layers have bores (47), which expose the land at a bottom of the bore, said land surrounding the opening of the hole in which a lead pin of the electronic part is to be inserted such that said bore communicates with the hole, and the lands connected to the wiring lines are covered with the insulation layer [claim 20].

Allowable Subject Matter

The indicated allowability of claims 6-11 is withdrawn in view of the newly discovered reference. Rejections based on the newly cited reference are stated above.

Response to Arguments

Applicant's arguments with respect to claims 2-4 and 6-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,400,573, granted to Mowatt et al., discloses mounting electronic parts to a core substrate having an outer insulation layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 703-306-5737. The examiner can normally be reached on Mon.-Th., 9AM - 6:30 PM and alt. Fri. 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-0725 for regular communications and 703-308-0725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JCSN
September 21, 2002

Albert W. Paladini 9-23-02
ALBERT W. PALADINI
PRIMARY EXAMINER